**Combinational Logic Circuits**

Question 1: Which one of the following set of gates are best suited for 'parity' checking and 'parity' generation.

A. NOR gate

B. AND, OR, NOT gates

C. EX-NOR or EX-OR gates

D. NAND gate

Answer: C

Question 2: The number of control lines for an 8 – to – 1 multiplexer is

2^n = 8

A. 2

B. 3

C. 4

D. 5

Answer: B

Question 3: The Gray code for decimal number 6 (0110)is equivalent to

A. 1100

B. 1001

C. 0101

D. 0110

Answer: C

Question 4: The logic circuit given below (Fig.1) converts a gray code y1y2 y3 into



A. Excess-3 code.

B. Binary code.

C. BCD code.

D. Hamming code

Answer: B

Question 5: The excess 3 code of decimal number 26 is

A. 0100 1001

B. 1000 1001

C. 0101 1001

D. 0100 1101

(Add 0011 to each BCD)

Answer: C

Question 6: The number of control lines for 32 to 1 multiplexer is

2^n = 32

A. 4

B. 5

C. 16

D. 6

Answer: B

Question 7: The logic function implemented by the circuit below is (ground implies a logic “0”)



I0 – 0 00 F = 0

I1 – 1 01 F = 1

I2 – 1 10 F = 1

I3 – 0 11 F = 0

A. F = AND (P,Q)

B. F = OR (P,Q)

C. F = XNOR (P,Q)

D. F = XOR (P,Q)

Answer: D

Question 8: The Boolean function f implemented in the figure using two input multiplexers is



F = E’0 + EA

F = EA

E = B’C + BC’

F = (B’C + BC’)A

F = AB’C + ABC’

A. 𝐴𝐵 ̅𝐶 + 𝐴𝐵𝐶

B. 𝐴𝐵𝐶 + 𝐴𝐵 ̅𝐶̅

C. 𝐴̅𝐵𝐶 + 𝐴̅𝐵 ̅𝐶

D. 𝐴𝐵̅̅̅̅𝐶 + 𝐴̅𝐵𝐶

E. None of the above

Answer: E

Question 9: The minimum number of 2-to-1 multiplexers required to realize a 4-to-1 multiplexer is

A. 1

B. 2

C. 3

D. 4

Answer: C

Question 10: how many 2 line to 4 line decoders are required to form 4 line to 16 line

A. 2

B. 3

C. 4

D. 5

Answer: D

Question 11: An encoder has 2^n inputs and n outputs.

A. True B. False

Answer: A